IFW 2133

Docket No.: GR 00 P 1969

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

By: Date: November 18, 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	09/864,980	Confirmation No: 3471
Applicant	:	Peter Aymar, et al.	
Filed	:	May 24, 2001	
Title	:	Device and Method to Carry Out a Viterbi-Algorithm	
Art Unit	:	2133	
Examiner	:	Fritz Alphonse	
Docket No.	:	GR 00 P 1969	
Customer No.	:	24131	

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97(C)(2)

Hon. Commissioner for Patents

S i r :

In accordance with 37 C.F.R. 1.97(c)(2) copies of the following patents and/or publications are submitted herewith:

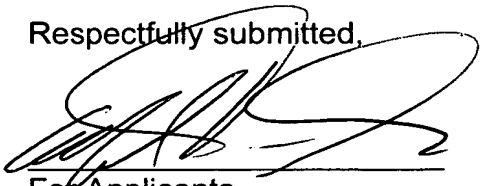
European Patent Application EP 0 944 173 A2 (Lee), dated September 22, 1999;

Biver, et al.: "Architectural Design and Realization of a Single-Chip Viterbi Decoder," 1989, 8220 Integration, the VLSI Journal, Amsterdam, NL, pp. 3-16.

In accordance with 37 C.F.R. 1.97 (c) (2), consideration of this Information Disclosure Statement is requested.

Enclosed is the fee in the amount of $180.00.

Respectfully submitted,



Alfred K. Dassler
52,794

For Applicants

Date: November 18, 2005

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101
/am

FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
GR 00 P 1969	09/864,980

Applicant: Peter Aymar, et al.

Filing Date	Group Art Unit
May 24, 2001	2133

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J	0 944 173 A2	9/1999	Europe				
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	Biver, et al.: "Architectural Design and Realization of a Single-Chip Viterbi Decoder," 1989, 8220 Integration, the VLSI Journal, Amsterdam, NL, pp. 3-16
	P	

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.